

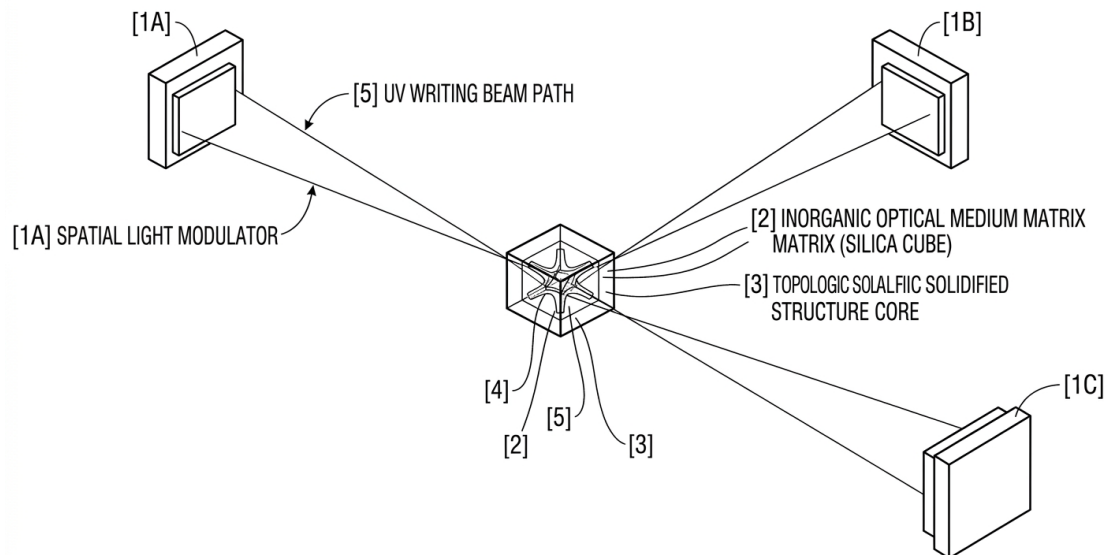
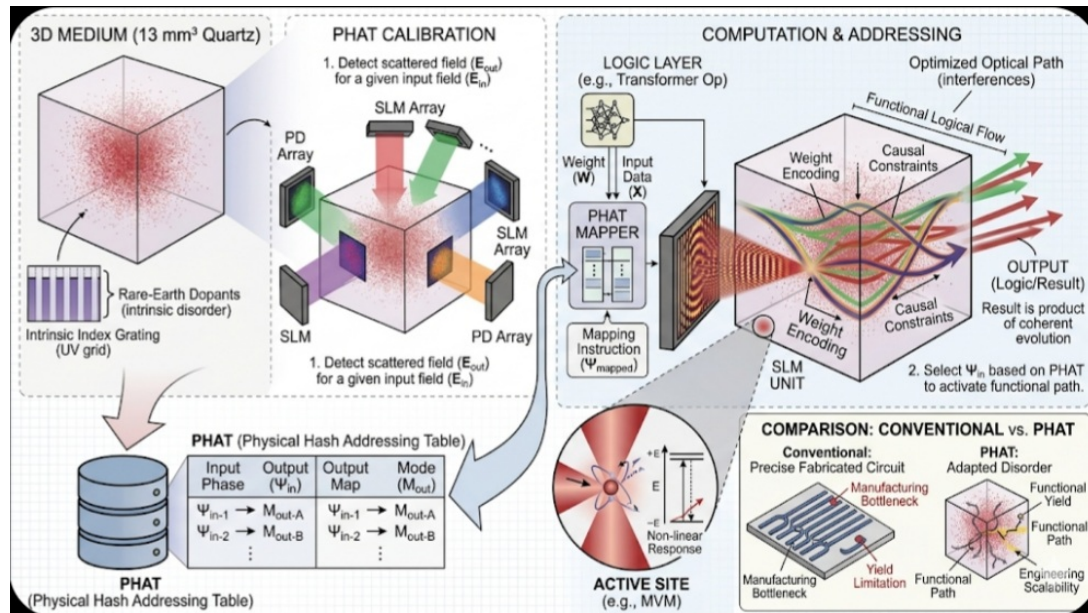
# B<sup>3</sup>D-HPA Continuous-Field Photonic Chip Architecture with Physical Hash Addressing

Version: V3.50

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## Abstract



From A to B, the photon traverses every possible path.

Phases interfere, waves superpose; the ultimate physical reality is simply the most

probable collapse of all spatial possibilities. To an observer, this may appear as brute-force traversal—yet it is nature’s own parallelism, unconstrained by clock cycles or data movement. In this work, we present the B<sup>3</sup>D-HPA architecture...

Precisely embedding computational logic into fused silica media represents the first critical threshold for continuous-wave optical computing to achieve engineering translation. Once overcome, its developmental pathway will become fully clear.

Traditional silicon-based chips and memory-computing architectures rely heavily on process scaling and structural uniformity. As physical limits are approached, they face insurmountable bottlenecks in power consumption, memory walls, cost escalation, and fabrication yield. Three-dimensional continuous-wave optical computing, with its inherent parallelism, low propagation loss, and wavefield interference computing capabilities, is regarded as a pivotal direction in the post-Moore era. However, inherent challenges including medium disorder, optical path stability, insufficient programmability, and sensitivity to thermal drift have long restricted its practical deployment.

This paper proposes the B<sup>3</sup>D-HPA (3D Body-High Performance Architecture), a continuous-wave optical computing architecture based on physical hash addressing. It employs rare-earth-doped fused silica as the core substrate, with sapphire (corundum) as an optional high-robustness medium, and uses active-passive hybrid coherent phase lattices formed by rare-earth ions as the system core. These phase lattices serve three critical functions: 3D coordinate anchoring, thermal drift sensing, and physical hash addressing (PHAT) seeding, laying a stable and reliable foundation for continuous-wave optical computing.

The architecture uses wavefield evolution and interference as its computing carrier. Through Physical Hash Mapping (PHM) and Physical Hash Address Tables (PHAT), it transforms inherent medium disorder from a defect into a native computational resource. Instead of pursuing absolute material uniformity, it utilizes scattering and refractive index distributions for algorithm-level adaptation.

One core innovation is Phase-Biased Heuristic Wavefield Collapse (A\*-like mechanism)\*: it maps the cost and bias concepts of heuristic pathfinding to optical wave propagation and interference. Path costs and heuristic guidance are physically encoded via phase accumulation, and optimal solutions emerge through constructive interference. This converts iterative digital search into a single-step physical parallel evolution, drastically reducing computational complexity and power consumption at the physical layer.

To address the key engineering challenges of optical field diffraction spreading and signal-to-noise ratio (SNR) degradation in continuous-wave optical computing, the architecture constructs 3D gradient-index (GRIN) virtual optical waveguide networks inside silica using ultraviolet cold-writing technology. Critically, rare-earth ions in silica do not act as discrete scattering particles, but form an effective continuous medium under the Effective Medium Theory (EMT): at 1550 nm or UV wavelengths, the ionic radius and

inter-ion spacing are orders of magnitude smaller than the optical wavelength, so light perceives a homogeneous medium with a globally modulated refractive index, rather than individual scattering centers. This enables the formation of invisible, boundaryless analog waveguides via UV-induced refractive index modulation ( $\Delta n$  typically  $10^{-3}$  to  $10^{-4}$ ), which outperform conventional etched silicon waveguides in key metrics: eliminating sidewall scattering loss, offering inherent mode matching with optical fibers, enabling dynamic reconfigurability, and delivering superior coherence and stability for continuous-wave computing. The self-focusing effect of near-parabolic refractive index profiles confines light fields within predefined topological paths, enabling directional, low-loss, high-energy-density optical signal transmission and significantly improving the SNR and modal stability of coherent computing. At the intersection of multiple waveguides, mode coupling and coherent superposition occur. The optical field interferes coherently according to phase differences, and optimal paths achieve strong energy localization via waveguide confinement, forming intense output signal peaks at constructive interference nodes to complete the physical collapse of heuristic optimal solutions. Leveraging photo-induced refractive index nonlinearity, the architecture further enables dynamic reconfiguration of 3D virtual waveguides. External control beams can in-situ generate and modify waveguide structures and adjust inter-waveguide coupling efficiency on nanosecond timescales, realizing real-time adaptation of hardware topology to computational tasks. This grants the system core advantages including in-situ online learning, unlimited hardware iteration, and physical-level encryption.

For real-world deployment, Version 3.50 establishes a five-layer thermal drift mitigation system:

1. Material-level low-drift substrates (silica / sapphire)
2. Architectural common-mode suppression
3. Sensor-level real-time backward feedback compensation via phase lattices
4. Algorithm-level relative phase invariance guarantee
5. System-level global calibration using pilot beams

This full set of mechanisms ensures stable operation in non-vacuum, non-thermostatic, and general industrial environments. It also supports UV cold write/erase reconfiguration, enabling reusable and reconfigurable optical computing hardware.

Version 3.50 is fully upgraded to an all-cold-state dual-level locking architecture, completely eliminating femtosecond laser structural ablation. Energy-level anchoring replaces physical damage, fundamentally eliminating thermal stress and lattice damage and reducing system failure rates to near zero. Through dual-level energy-layer separation, it achieves an erasable self-healing "bone-skin" logic structure: deep energy levels ("bone") correspond to stable inference states with near-immutable states; shallow levels ("skin") correspond to training/reconfiguration states supporting flexible rewriting. On this basis, the architecture supports three configurable modes: fully erasable,

bone-skin hybrid, and fully non-erasable, covering applications ranging from flexible general computing to high-security fixed-function systems.

B<sup>3</sup>D-HPA decouples computational correctness from physical uniformity, allowing disordered media to serve as reliable computing substrates. With thermal drift systematically suppressed, remaining engineering challenges no longer constitute fundamental obstacles, providing a mass-producible, scalable, and practical pathway for continuous-wave optical computing.

## 1 Introduction

Traditional digital computing systems rely on highly regular device structures and precise timing control. As fabrication processes approach atomic scales, performance gains are severely constrained by thermal issues, interconnect latency, and manufacturing costs. Continuous-wave optical computing performs computations via parallel propagation and interference of 3D wavefields, offering inherent advantages in low power consumption, high parallelism, and noise immunity. However, it has long been hindered by five practical barriers:

1. Internal medium disorder and scattering cause non-reproducible and fluctuating computation results.
2. Optical path drift induced by temperature and stress destabilizes phase and interference states.
3. Lack of stable, low-power real-time calibration and compensation mechanisms.
4. Weak programmability and reconfigurability, limiting adaptation to real tasks.
5. Insufficient 3D writing SNR and limited throughput, restricting the engineering realization of 3D optical storage and computing.

B<sup>3</sup>D-HPA V3.50 completely abandons the pursuit of perfectly uniform materials and instead constructs a systematic framework centered on phase lattices for sensing, physical hash for addressing, relative phase for computational invariance, and cross hybrid writing for engineering reliability. By embedding rare-earth phase lattices into 3D media, the system gains distributed in-situ sensing and coordinate references. Physical hash addressing converts inherent microscopic variations into reusable physical fingerprints. Relative phase invariance ensures global perturbations do not disrupt computational logic. Multi-mode hybrid writing fundamentally resolves the SNR and throughput bottlenecks that have plagued the field for decades.

V3.50 further introduces key architectural refinements: all-cold-state dual-level locking replaces femtosecond physical ablation, separating permanent backbone and dynamic modulation via energy depth differences, completely eliminating structural damage and thermal drift risks. By adjusting energy depth configurations, the system can operate in fully erasable, bone-skin hybrid, or fully non-erasable modes, greatly expanding engineering applicability.

Final Goal:

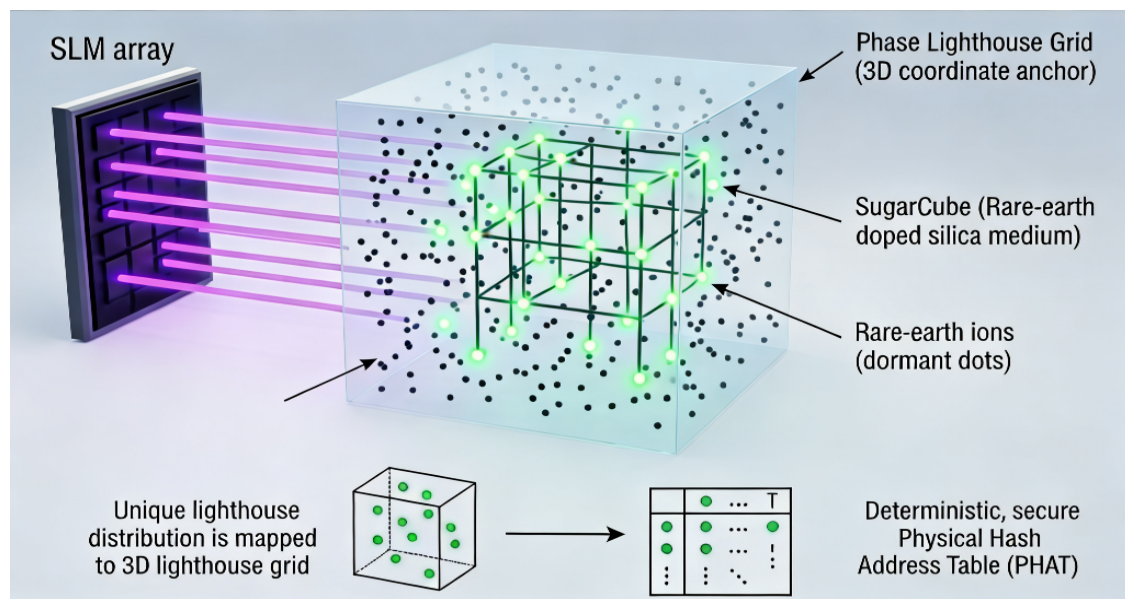
To realize mass-producible, stably operating, and dynamically upgradable continuous-wave optical computing chips in non-laboratory environments.

## 2 Fundamentals of Continuous-Wave Optical Computing and 3D Media

Computational power originates from coherent propagation and interference evolution of 3D continuous optical fields inside doped media. Amplitude, phase, wavelength, and polarization of incident light collectively define the global electromagnetic field distribution. Multi-path superposition, mode coupling, and phase modulation jointly implement tensor-like parallel operations.

Unlike the discrete gate-level architecture of digital circuits, continuous-wave computing operates in a fully parallel, clock-free, data-movement-free manner, offering fundamental advantages in bandwidth and power efficiency.

### 2.1 Physical Hash Mapping (PHM)



Physical Hash Mapping establishes a stable correspondence between random scattering responses of the medium and deterministic logical addresses. Its core principles are:

- Medium disorder is not treated as error but as indexable physical computational resource.
- Even with microstructural differences between chips, consistent logical behavior is achieved via stable individual PHATs.

This breaks the dependency of optical computing on ultra-high-precision uniform fabrication, enabling engineering translation.

### 2.2 Three-Layer Mechanism of Physical Hash Addressing

PHAT operates across physical, address, and logical layers:

#### 2.2.1 Physical Layer: Intrinsic Response Sampling

- SLM array emits orthogonal calibration fields.

- Detectors record scattering and interference outputs.
- Rare-earth phase lattices provide high-contrast backward reference signals, forming a unique optical fingerprint for each chip.

This layer defines the physical identity of the chip.

#### 2.2.2 Address Layer: Spatial Hashing of Responses

- Phase lattice positions serve as natural anchor points.
- Continuous optical fields are discretized into stable address entries to form the PHAT.
- Mapping from disordered medium to structured address space is realized.

#### 2.2.3 Logical Layer: Dynamic Address-Logic Binding

During inference, PHM maps logical operations to optimal physical paths:

- SLM loads phase distributions according to PHAT.
- Optical fields evolve along stable, low-loss channels.
- Phase lattices provide real-time alignment and compensation references.

### 2.3 SugarCube Carrier Concept

“SugarCube” denotes only the initial experimental cubic form. The architecture natively supports arbitrary 3D geometries including spheres, hemispheres, irregular volumes, and brain-like dendritic morphologies, fully exploiting the inherent parallelism of continuous-wave propagation.

#### 2.4 Substrate Selection: Fused Silica and Sapphire

- Fused silica: low cost, low optical loss, low thermo-optic coefficient, suitable for mass production and consumer applications.
- Sapphire: higher thermal conductivity, stronger resilience to stress and temperature, suitable for extreme environments and high-reliability scenarios.

Common feature:

Thermal drift appears as global, low-dimensional, approximately common-mode perturbation, which enables low-complexity closed-loop compensation.

Comparison with silicon:

- Silicon exhibits strong thermo-optic effects and severe local hotspots, leading to high-dimensional disordered perturbations.
- Complex inverse scattering solutions are required, inevitably causing computational overhead inversion.

Material is algorithm: physical properties of substrates directly determine the complexity and engineering feasibility of system compensation architectures.

Optional pre-doping enhancement scheme:

As an optional engineering enhancement, dopants with tailored thermo-optic and photosensitive properties can be introduced during substrate fabrication. Since directly embedding regular nanowaveguides during silica growth is difficult and lacks consistency, the architecture adopts a more industrially viable strategy: instead of forming fixed waveguide profiles upfront, a uniform doping system is pre-deposited that

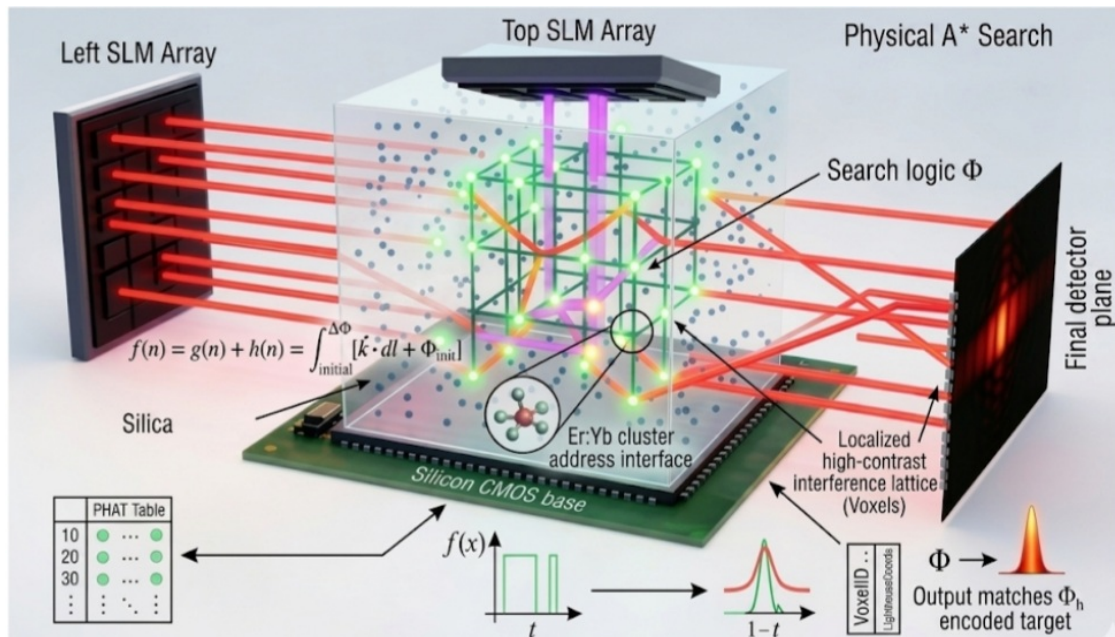
significantly lowers waveguide writing thresholds and provides thermal drift compensation.

Such dopants can be chosen to have opposite thermo-optic coefficients relative to the host, creating physical cancellation of refractive index changes under temperature variations and improving overall optical path thermal stability. Doped regions also exhibit stronger photo-induced refractive index response, enabling more efficient, lower-power UV cold writing of 3D virtual waveguide networks with clearer confinement and lower propagation loss.

This pre-doping strategy is optional and not mandatory, allowing flexible adoption based on application scenarios, cost budgets, and process conditions.

### 3 Phase-Biased Heuristic Wavefield Collapse (A\*-like Mechanism)

#### 3.1 Physical Mapping of Heuristic Optimization



Cost and heuristic functions in pathfinding are mapped to optical path phase accumulation:

- Path cost  $g(n) \rightarrow$  propagation phase delay
- Heuristic bias  $h(n) \rightarrow$  SLM-programmed spatial phase distribution

Optical fields evolve in parallel, and optimal paths emerge naturally as constructive interference peaks, with one physical step equivalent to tens of thousands of digital iterations.

To mitigate diffraction spreading and SNR degradation, UV cold-writing creates 3D GRIN virtual waveguide networks. Critically, rare-earth ions in silica operate as an effective continuous medium under the Effective Medium Theory (EMT): at 1550 nm or UV wavelengths, the ionic radius ( $\sim 0.1$  nm) and inter-ion spacing are 1000–10000 times smaller than the optical wavelength, so light perceives a homogeneous medium with a globally modulated refractive index, rather than individual scattering particles. This

enables the formation of invisible, boundaryless analog waveguides via UV-induced refractive index modulation ( $\Delta n$  typically  $10^{-3}$  to  $10^{-4}$ ), which outperform conventional etched silicon waveguides in key metrics: eliminating sidewall scattering loss, offering inherent mode matching with optical fibers, enabling dynamic reconfigurability, and delivering superior coherence and stability for continuous-wave computing. Parabolic-like index profiles provide self-focusing, confining light to predefined paths for directional, low-loss, high-density transmission and suppressing speckle while preserving coherence. Light intensity control enables precise index modulation, which must strictly match topological blueprints for heuristic collapse or single-shot full-layer writing. While intensity-based index modulation is a physical means, matching modulation profiles to computational topologies is what transforms raw silica into intelligent computing chips. Within the heuristic physical framework, the cost distribution  $f(n) \sim g(n) + h(n)$  exists physically as a 3D refractive index landscape:  $g(n)$  corresponds to the foundational index backbone, with phase accumulation representing path cost;  $h(n)$  corresponds to SLM-imprinted auxiliary index gradients that physically guide photons toward optimal solutions. Upon coherent injection, the field automatically forms maximally constructive interference paths, enabling instantaneous physical solution of heuristic optimization problems.

At waveguide intersections, mode coupling and coherent superposition occur. Optimal paths concentrate energy via waveguide confinement, producing strong output peaks at constructive interference nodes to complete physical wavefield collapse. Unlike silicon electronics that shuttle electrons through metal wires, B<sup>3</sup>D-HPA guides light via refractive index barriers, enabling wiring-free, 3D, self-aligned all-optical computing. Waveguide structures exhibit inherent geometric robustness to small stress disturbances: minor thermal deformation of silica leaves energy-locked relative positions unchanged, maintaining stable guiding performance.

Via photo-induced nonlinearity, 3D virtual waveguides support dynamic reconfiguration: external control beams generate, modify, and adjust coupling on nanosecond scales, adapting hardware topology to tasks in real time. This enables in-situ learning, unlimited hardware evolution, and physical-layer encryption, supporting long-term advancement of continuous-wave optical computing.

Weight adjustment is realized via evanescent field coupling between closely spaced but non-contacting waveguides. By fine-tuning the refractive index of the medium between waveguides through UV cold writing, the photon transfer ratio can be precisely controlled. This ratio physically encodes the synaptic weight in neural networks: a higher weight allows stronger signal transmission, while a lower weight suppresses it.

Short-term plasticity is supported by metastable energy levels of rare-earth ions, enabling temporary weight tuning on timescales of seconds to minutes, analogous to working memory. Long-term plasticity is achieved via deep-level energy locking, which

permanently consolidates learned weights within the silica matrix.

A core engineering advantage of the B<sup>3</sup>D-HPA V3.50 architecture lies in its 3D gradient-index (GRIN) virtual optical waveguide design, which achieves an optimal balance between single-mode precision and micron-scale mechanical robustness. Unlike silicon nanowaveguides that suffer from severe thermal drift, evanescent crosstalk, and stress-induced leakage, or silicon microwaveguides plagued by modal dispersion and prohibitive bending radii, the GRIN virtual waveguide in fused silica leverages a near-parabolic refractive index profile to confine light fields tightly within a central "nanoscale core" while maintaining a micron-scale physical footprint. This structure inherently eliminates multi-modal dispersion, ensuring pure single-mode transmission with sharp, distortion-free logic signals. The monolithic integration of waveguides within the silica medium eliminates mechanical stress, optical leakage, and inter-waveguide crosstalk, while the ultra-low thermo-optic coefficient of silica provides intrinsic thermal stability without active compensation. The 3D spatial freedom of the SugarCube platform further enables dense, low-crosstalk waveguide routing with relaxed bending radius requirements, delivering logic density that outperforms 2D silicon nanowaveguides while retaining the robustness of micron-scale structures.

At computational nodes where multiple waveguide synapses converge, optical fields undergo linear superposition followed by coherent collapse through constructive or destructive interference. This process natively implements weighted summation (MAC) and activation functions with extremely low energy dissipation. The entire operation completes instantaneously during wavefront propagation, without transistor switching or sequential electronic operations.

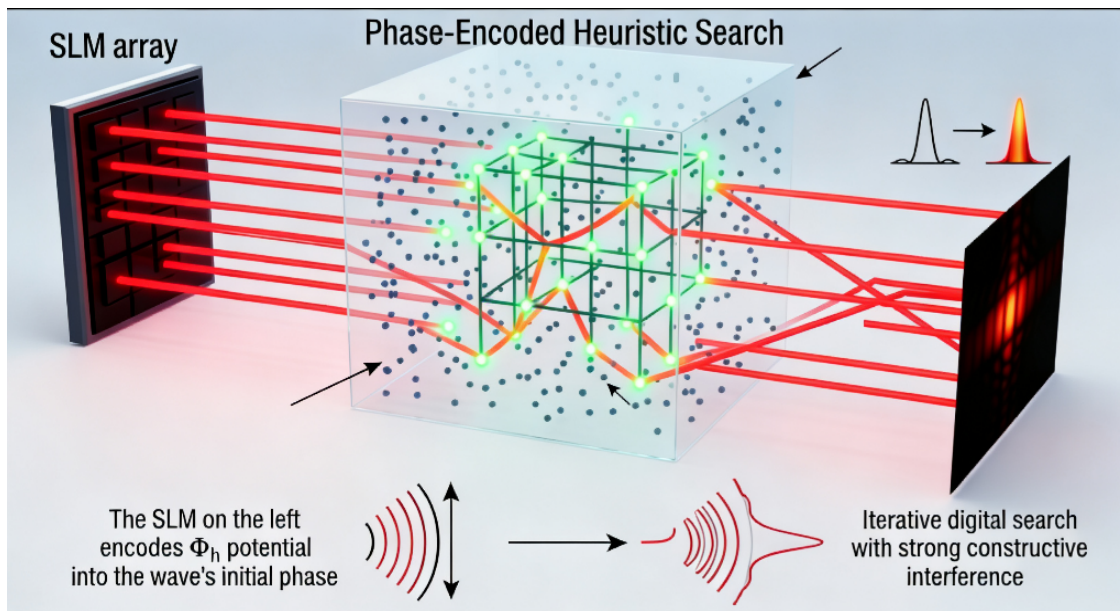
### 3.2 Relative Phase: Foundation of Computational Invariance

All logical decisions rely only on relative phase differences, not absolute phase.

Global phase shifts from temperature or stress are common-mode perturbations that preserve relative relationships and thus computational results.

This is the core anti-drift principle of the architecture.

### 3.3 Interference Selection Mechanism



- Low total phase path  $\rightarrow$  constructive interference  $\rightarrow$  intensity peak

- High total phase path  $\rightarrow$  destructive interference  $\rightarrow$  weak intensity

Output intensity distribution directly encodes optimal solutions without complex post-processing.

### 3.4 Phase Anchoring and Stability

Phase lattices form a 3D distributed reference grid, providing real-time phase error signals to the SLM for analog closed-loop stabilization without high-speed digital signal processing.

## 4 Core Mechanisms of Physical Hash Addressing (PHAT)

### 4.1 3D Refractive Index Grid Preparation and Multi-Mode Writing Processes

UV dual-wavelength pumping enables cold writing and erasure without femtosecond ablation, supporting repeated reconfiguration and low-damage, reusable phase lattice grids. The architecture integrates three complementary writing modes and three erasability levels, forming a complete and scalable engineering system.

#### 4.1.1 Point-by-Point Writing: Laboratory-Grade Physical Sovereign Calibration

Point-by-point writing uses high-precision SLMs to modulate voxel-wise refractive indices like embroidery, with every phase shift refined via hash tables. This establishes the "physical sovereignty" of the architecture, calibrating core logic units and verifying physical parameters. Though time-consuming, it defines the architecture's precision ceiling.

#### 4.1.2 Depth-Progressive Writing: Industrial Dynamic Growth Process

Depth-progressive writing uses lateral scanning lines (optical blades) for layer-wise activation, synchronized with vertical infrared SLMs. It supports adaptive "write-inspect-compensate" calibration, balancing precision and speed, serving as the

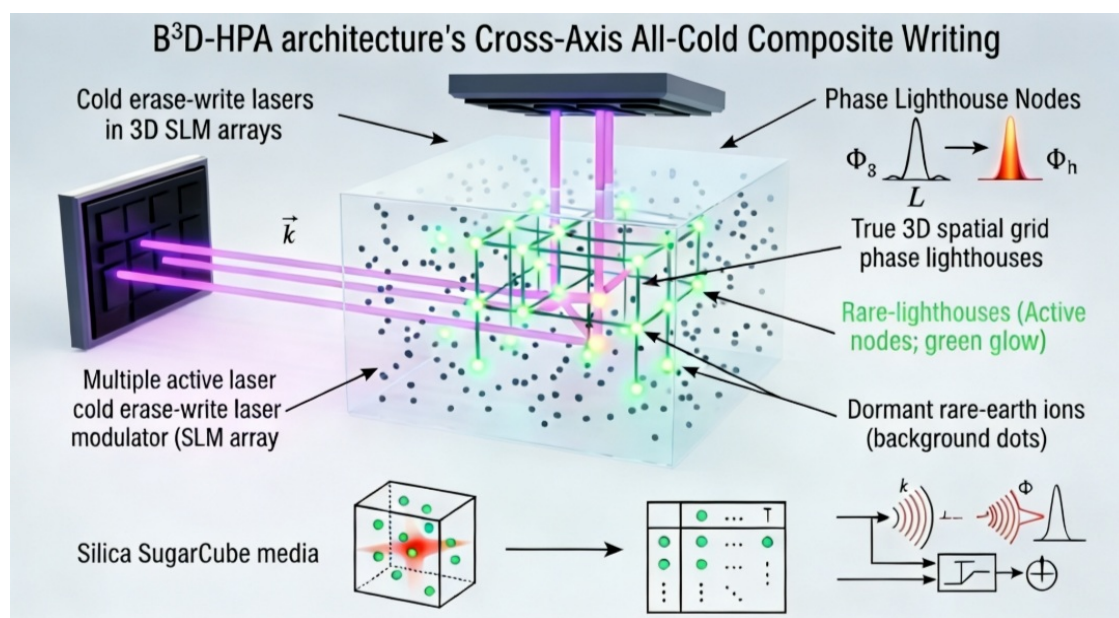
core pathway for high-throughput chip mass production and resolving yield issues in complex 3D structures.

#### 4.1.3 Single-Shot Full-Layer Writing: Mass-Producible Inclusive Computing Solution

Single-shot full-layer writing uses lateral UV area sources for global layer activation, synchronized with vertical SLMs to complete full-stack writing in one pass. It converts microphysical writing into macro “photocopying” operations, setting the baseline for mass production and enabling copy-machine-level scalability for photonic chips.

High-precision energy mapping by SLMs is required. For nonlinear responses from rare-earth ion transitions, the writing system employs nonlinear pre-compensation based on medium energy-index conversion tensors to invert required UV intensity profiles from target indices. Global holographic alignment calculates 3D holographic energy distributions via full-field superposition, dynamically adjusting UV power using PHAT-derived medium inhomogeneity data to cancel intrinsic defects and strictly match algorithmic topologies.

#### 4.1.4 Cross Hybrid Writing: Industrial Holographic Printing System



The architecture introduces a cross hybrid writing scheme as the ultimate fabrication solution, integrating all three modes in one chamber to form an industrial holographic printer:

- Vertical axis area sources / tomographic scanning: rapidly lay down foundational logic (PHAT indices, physical constraints), completing 90% of weighting in parallel for high throughput.
- Lateral axis parallel SLM UV arrays: act as “logic correctors”, performing secondary energy-level boosting on targeted rare-earth sites to refine residuals point-by-plane after coarse writing.
- Cross-locking addressing: orthogonal vertical and lateral optical paths form

high-contrast energy lattices, minimizing off-target excitation and eliminating writing crosstalk.

This “coarse-then-fine, write-as-you-inspect” process achieves both area-source throughput and SLM-level precision, with hybrid-field holographic error correction pushing yields near 100%, solving three fundamental bottlenecks of 3D optical writing:

1. Writing SNR: non-coaxial side pumping ensures inactive layers remain unexposed, enabling layer-isolated writing without strict interferometric fringe stability.
2. Throughput: area-source single-shot writing achieves parallelism beyond silicon etching, escaping lab-scale point-by-point limits.
3. 3D addressing precision: cross mechanism enables true 3D physical addressing balancing speed and accuracy for practical 3D optical storage and computing.

In conventional displays and lithography, SLMs are limited by millisecond-scale liquid crystal response or MEMS flipping rates. Such criticisms rely on a “frame-scanning” mindset. In B<sup>3</sup>D-HPA V3.50, SLM usage undergoes a paradigm shift that amplifies its engineering value in three dimensions:

1. From “prime mover” to “steering wheel”: computation does not occur in the SLM  
Silicon-centric thinking assumes SLMs must refresh per frame like CPU clocks. In V3.50, computation proceeds via continuous lightwave interference at the speed of light; SLMs only configure the environment. Once phase profiles are loaded via PHAT, interference logic persists stably without refresh. SLMs are only activated for model switching or drift compensation, separating configuration and runtime states and fundamentally eliminating reliance on SLM refresh rates.

2. Spatial freedom as superpower: trading area for time

Although SLM refresh rates lie in the kHz range, their spatial bandwidth (pixel count) is enormous. A single 4K SLM provides ~8 million independent modulation elements, which via 3D interference effectively drive billions of virtual logic gates in parallel. Silicon CPUs rely on high-frequency serial execution; silica chips achieve instantaneous result collapse via massive spatial parallelism, enabling AGI-scale throughput even with low-frequency SLMs.

3. Relief via hybrid writing: the salvation of cross architecture

Cross hybrid writing unburdens SLMs: area sources handle 90% of static backbone writing, while SLMs only refine 10% of dynamic logic. For ultra-high-speed signal applications, coherent mixing is used: SLMs provide static carrier phase anchors, and GHz-bandwidth external EOMs perform high-speed modulation, further reducing SLM frequency demands.

#### 4.1.5 Erasability Levels and Application Scenarios

Based on locking depth and relaxation lifetime of rare-earth energy levels, the architecture supports three UV-compatible erasability modes:

1. Fully erasable mode: shallow metastable levels, full-area UV erasure and full

reconfiguration. Suitable for research platforms, rapidly iterated algorithms, and reconfigurable intelligent hardware.

2. Bone-skin hybrid mode (semi-erasable): dual-level locking separates permanent backbone (deep levels, inference) and dynamic logic (shallow levels, training/reconfiguration). Balances stability and runtime programmability, ideal for mainstream industrial photonic chips.

3. Fully non-erasable mode: deep potential wells written once with lifetimes of years to decades, resistant to external tampering. Suitable for high-security fixed-function systems, critical infrastructure controllers, and hardware root-of-trust modules.

#### 4.2 Optical Fingerprint Calibration

Each chip carries a unique optical fingerprint from random natural rare-earth distribution:

- Serves as the basis for PHAT generation.
- Enables physical anti-counterfeiting and anti-cloning.
- Ensures consistent logical behavior across chips despite material variations.

#### 4.3 Runtime Dynamic Mapping and Path Activation

PHAT delivers optimal wavefront configurations to the SLM:

- Optical fields self-evolve in the medium.
- Backward lattice signals correct drift in real time.
- Enables dynamic, adaptive, evolvable optical computing paths.

#### 4.4 Cold Write/Erase Reconfiguration

UV excitation locally resets metastable rare-earth levels, enabling:

- Online updating of weights, biases, and topological paths.
- FPGA-like programmable photonic hardware.
- Sustained adaptation to new tasks and environments.

### 5 Five-Layer Thermal Drift Mitigation Architecture

#### 5.1 Material-Level Stability

Silica and sapphire feature low thermal expansion and thermo-optic coefficients:

- Reduces drift magnitude at the source.
- Eases subsequent compensation burden.

#### 5.2 Architectural Common-Mode Suppression

Monolithic homogeneous media make global perturbations highly correlated:

- Relative differences remain stable.
- Provides physical foundation for relative-phase computing.

#### 5.3 Sensor-Level Real-Time Compensation

Backward signals from phase lattices enable distributed in-situ drift sensing:

- Real-time SLM compensation.
- End-to-end phase closed loop.

#### 5.4 Algorithm-Level Invariance

Relative phase differences are immune to global perturbations:

- Computational stability persists despite absolute phase drift.
- Forms the fundamental guarantee of environmental robustness.

### 5.5 System-Level Pilot Beam Compensation

Dedicated pilot beam injection:

- Monitors global phase shift.
- Maintains stable interference patterns via PLL-style closed loops.
- Avoids inverse scattering; only global phase correction.
- Achieves constant-time  $O(1)$  stabilization.

## 11 Mitigation of Key Engineering Barriers

### 11.1 Dimensionality Reduction and Closed-Loop Control for Inverse Scattering

Traditional optical compensation often falls into high-dimensional inverse scattering traps:

- Attempting to invert global multi-path scattering matrices from output distortions.
- Leads to exponential explosion in compensation complexity and computational overhead inversion.

$B^3D$ -HPA avoids reconstructing internal scattering paths: This architectural advantage is further highlighted by the fundamental limitations of silicon-based photonic waveguides, which are trapped in an unavoidable trade-off between nanoscale integration and micron-scale stability. Silicon nanowaveguides, despite their high integration density, suffer from catastrophic thermal drift, evanescent field crosstalk, and extinction ratio collapse, requiring power-intensive active thermal compensation that negates the low-power benefit of photonic computing. Silicon microwaveguides, while mechanically stable, introduce severe modal dispersion that distorts logic signals and requires impractically large bending radii, making high-density integration impossible. In contrast, the GRIN virtual waveguide in  $B^3D$ -HPA transcends this trade-off entirely, enabled by the Effective Medium Theory (EMT) of rare-earth-doped silica: rare-earth ions act as a continuous effective medium rather than discrete scatterers, allowing the formation of boundaryless analog waveguides that achieve single-mode precision through refractive index confinement, micron-scale mechanical robustness through material stability, and unlimited integration density through 3D spatial routing, eliminating all core physical bottlenecks of silicon photonic architectures at the source. Uses relative phase invariance, taking only phase lattice feedback as reference.

- Applies global or low-gradient phase shifts via PLL logic.
- Reduces high-dimensional inverse problems to constant-time  $O(1)$  closed-loop negative feedback regulation.

### 11.2 Coherent Signal Extraction in Strong Scattering Backgrounds

Core challenge:

- Reliably extracting weak backward echoes from rare-earth phase lattices under intense primary scattering fields.

Conventional intensity detection imposes excessive dynamic range demands:

- Weak signals are submerged.
- Engineering implementation infeasible.

This architecture introduces heterodyne mixing and coherent lock-in amplification:

- Pilot beams are encoded with unique microwave offsets or phase modulation signatures.
- Detectors use local oscillator references.
- Coherent heterodyning shifts weak phase features to low-frequency electrical signals.
- Broadband unmodulated noise from primary fields is filtered out.
- Enables robust extraction “in storm-level scattering” without extreme-dynamic-range sensors.

### 11.3 Physical State Preservation and All-Cold Dual-Level Self-Healing Architecture

To address yield loss and residual stress drift from femtosecond processing, B<sup>3</sup>D-HPA V3.50 fully eliminates destructive physical machining. The system uses Deep-Level Locking instead of structural fixation.

This architecture exploits asymmetric relaxation of rare-earth 4f–5d orbital levels:

- Base topological layer: high-potential metastable levels form permanent index grids via threshold-specific UV excitation.
- Dynamic modulation layer: shallow-potential levels support logical rewriting and programmability.

This fully coherent cold process ensures uniform internal stress. Under temperature fluctuations, silica expands homogeneously, and phase shifts are perfectly corrected by O(1) closed-loop feedback, free from nonlinear high-dimensional drift induced by femtosecond damage.

V3.50 redefines bone-skin logic via dual-level locking and extends to three erasability modes:

- Deep anchored state (bone): high-power narrow-pulse UV writing, multiyear relaxation, defining PHAT origin and foundational paths.
- Shallow modulated state (skin): low-power wide-pulse writing, short relaxation, for real-time weight alignment, path trimming, and parameter compensation.

Selective full-shallow, hybrid, or full-deep writing enables fully erasable, hybrid, or fully non-erasable operation for diverse security and flexibility needs.

Self-healing logic:

Periodic in-situ non-destructive rewriting of deep states via shallow channels maintains long-term stability, eliminating structural aging and thermal drift from femtosecond processing.

### 11.4 PHAT Table Size Control

Sparse anchor coding, local hash compression, and learned indexing keep tables within MB-scale for real-time performance. Hierarchical partitioned addressing supports scaling without memory bottlenecks.

#### 11.5 SLM Bandwidth Demand and Writing Computational Efficiency

One-shot calibration plus low-frequency drift compensation drastically reduces SLM throughput requirements. Coarse-fine hybrid writing further reduces refresh pressure by an order of magnitude, matching industrial mass production.

Crucially, the architecture resolves writing computational efficiency across physical, algorithmic, and system layers, eliminating the paradox of “spending more computing to make a computer”.

##### 11.5.1 Physical Layer: From Logical Equation-Solving to Geometric Alignment

Traditional 3D holographic storage and optical computing suffer crippling overhead due to high-dimensional inverse scattering: full-path multi-scattering inversion per voxel leads to exponential complexity and overhead inversion.

B<sup>3</sup>D-HPA abandons inverse scattering, reducing writing to minimal geometric alignment:

- Single-shot area writing: near-zero computing. Predefined masks or static phase maps loaded once to SLMs, with global area-source activation for full-layer writing without real-time computation or iteration: true macro-photocopy operation.
- Depth-progressive writing: ultra-low computing. Linear SLM timing along predefined paths with low-dimensional closed-loop residual compensation, constant  $O(1)$  complexity without exponential growth.
- SLM parallel refinement: controllable computing. Only 10% of post-coarse-writing voxels require local phase trimming, no global recalculation,  $\sim 1/10$  load of point-by-point writing.

##### 11.5.2 Algorithmic Layer: One-Calibration, Lifetime-Reuse PHAT

Physical Hash Address Tables enable amortized computing cost:

- One-time offline optical fingerprint sampling and PHAT generation during chip production.
- All subsequent writing, reconfiguration, and compensation reuse pre-calibrated PHAT, avoiding repeated scattering inversion with constant-complexity address-logic mapping.
- Functional upgrades only require partial PHAT updates, not full recalibration, maintaining minimal cost.

##### 11.5.3 System Layer: Computational Hierarchical Optimization via Hybrid Writing

Cross hybrid writing enables optimal computing partitioning:

- 90% of foundational logic written in parallel via area sources with near-zero computing.
- Only 10% of precision refinement handled by SLMs, concentrating effort on critical regions and eliminating global waste.
- Entire flow avoids high-speed DSP, relying only on low-frequency, low-bandwidth SLM control and closed-loop compensation, with computing load far below silicon chip manufacturing.

This ensures writing is computationally “cheap”, validating mass-production viability: optical computing performance is not negated by fabrication overhead, realizing truly low-power, high-parallelism, low-cost computing.

#### 11.6 Computational Accuracy Assurance

Multi-path voting, output calibration matrices, and confidence filtering suppress phase noise for bounded engineering-grade error. Holographic error correction in cross hybrid writing further pushes writing precision and yield to industrial standards.

### 6 Optoelectronic Interface and Digital Reconstruction Layer

#### 6.1 Physical Quantization: From Probabilistic Wavefields to Digital Signals

Photon incidence on PD arrays at the SugarCube output represents collapse and quantization from analog physics to digital signals:

- Phase distribution, interference texture, spatial intensity → photoelectric effect → current pulses.
- Maps continuous physical quantities to discrete electrical signals.

#### 6.2 High-Parallel Output and Array Sampling

A key advantage of SugarCube is full-parallel computing output:

- Not serial bit-by-bit transmission.
- Large-scale PD arrays (e.g., 4096×4092) sample synchronously.
- Full results captured in single exposure.
- Equivalent to collecting final states of trillions of physical evolutions at once.

#### 6.3 PHAT Translation and Logical Alignment

Conventional von Neumann systems cannot natively digest ultra-high-bandwidth parallel optical outputs:

- Raw PD data is logically aligned via PHAT.
- Physical hash tables act as translators to the digital domain.
- Binds intensity peaks, spatial modes, and computational semantics.
- Assigns clear logical meaning and optimal solution labels to each detector channel.

#### 6.4 Hybrid Silicon-Photonics Architecture

The system adopts heterogeneous silicon-photonics collaborative computing:

- Silicon CPU/MCU: user interaction, protocol handling, instruction decoding, task scheduling, serial logic.
- Silica OPU (Optical Processing Unit) / TPU (Topological Processing Unit): raw high-parallelism computing, physical evolution, interference emergence.
- Net efficiency gains across layers if optical savings exceed ADC/DAC overhead.

#### 6.5 Hybrid Mode: Discrete Timed Logic and Continuous-Wave Computing

In conventional understanding, continuous-wave optics and digital timing represent opposing paradigms: clock-free parallel interference vs. clocked gate-sequential execution. Mapping CPU timing directly into waveguides, while functionally possible,

strangles parallel advantages by confining 3D physics into low-dimensional digital timing. Crucially, B<sup>3</sup>D-HPA supports asymmetric hybrid operation, not replacement:

- Discrete timed paths (static/semi-static waveguides) handle scheduling, boundary constraints, state latching, and protocol handshake, ensuring compatibility with digital instruction sets.
- Continuous-wave regions (dynamically indexed landscapes) perform high-parallelism, high-complexity, emergent tasks: pathfinding, tensor transformation, interference decision-making.

Timed paths do not execute core logic; they control injection timing, spatial partitioning, and result gating. Continuous-wave domains operate clock-free, solving problems instantaneously via physical evolution and feeding intensity patterns back to trigger next states.

Coexisting in 3D space, functionally decoupled, asynchronously coupled, they form a hybrid control-compute system.

This relieves the von Neumann bottleneck: instructions, memory, and computing distribute volumetrically without long-distance data movement. Timed logic ensures determinism; continuous waves deliver efficiency. Compared to 2D silicon stacking of control and compute, 3D silica offers inherent spatial separation, providing a foundational heterogeneous paradigm for post-Moore computing.

## 7 Typical Application: Physical-Light 3D Rendering and Ray Tracing

### 7.1 Fundamental Difference Between GPU and Photonic Computing

Conventional GPUs perform ray tracing numerically via BVH traversal:

- Discrete arithmetic emulates continuous physics.
- Computationally heavy, high-latency, power-hungry.

In silica photonic chips, ray tracing is not numerical:

- It is direct physical propagation, reflection, refraction, and interference of photons.
- Refractive index landscapes directly encode scene geometry and lighting.

### 7.2 Physical Ray Tracing Implementation

UV cold-writing imprints 3D scene geometry as index landscapes inside silica:

- Upon injection, photon propagation natively performs full ray tracing.
- PD arrays capture output intensity distributions.
- Single-shot frames include ambient occlusion, global illumination, and refraction.
- No intermediate ray data streaming; only final frame buffer output.

### 7.3 Zero-Latency Interactive Response

Camera motion corresponds to incident angle variation:

- Relative-phase adaptation enables instantaneous interference restructuring.
- PD arrays output updated frames in real time.
- Response limited only by physics, far exceeding GPU performance.

## 7.4 Hardware and Power Efficiency

No massive cores or VRAM required:

- Scene and texture stored distributedly as index gradients.
- Power drops from hundreds of watts to watt-scale or below.
- Negligible heat, ideal for edge and embedded systems.

## 8 Extended Features: Physical Observability and Optical Storage

### 8.1 Physical-Layer Debugging and Interpretability

Lateral scattering or thin-film interference enables real-time monitoring of internal wavefields:

- Full physical observability of computation.
- Faults localized to phase distortions or energy-level defects.
- Corrected via localized UV pumping.
- Higher transparency and debuggability than neural network black boxes.

### 8.2 Derivative: Silica Photonic Solid-State Storage

Rare-earth-doped silica directly serves as non-volatile optical storage:

- UV-written energy-level states retain data long-term.
- Low-power, highly stable, interference-resistant photonic SSDs.
- Integrated storage-computing as derivative hardware.
- Cross hybrid writing resolves stability and throughput limitations of conventional holography, enabling next-generation high-capacity, reliable, mass-producible storage.

## 9 Operational Mechanisms and Engineering Properties

### 9.1 Non-Volatile Physical Storage

UV-programmed metastable states preserve phase profiles:

- Data retention without power.
- Non-volatile computational substrates.
- Supports long-term offline operation.

### 9.2 Defect Adaptation and Anchor Pruning

System automatically discards weak-response lattices:

- Maintains robustness.
- Prevents local defects from breaking global function.

### 9.3 Path Rotation and Lifetime Balancing

PHAT enables equivalent-path rotation:

- Avoids localized aging and fatigue.
- Extends hardware lifetime.

### 9.4 Physical Uniqueness and Security

Unique optical fingerprint per chip:

- Enables hardware authentication.

- Anti-cloning and anti-tampering.
- Inherent hardware root of trust.

#### 10 Paradigm Shift: Structure Is Model, Propagation Is Computation

In GPU/TPU:

Computation = Instruction fetch + Scheduling + Data movement

In B<sup>3</sup>D-HPA:

Computation = Wavefield injection + Natural propagation + Interference emergence

Clock-free, bus-free, cache-free:

the von Neumann bottleneck is fundamentally broken.

#### 12 Mass-Production Potential and Engineering Value

Traditional optical computing demands ultra-precise, uniform, stable fabrication and environments, resulting in prohibitive cost and low yield.

B<sup>3</sup>D-HPA redefines yield: a chip is valid if phase lattice signals are stably detectable.

Substrates, SLMs, and detectors use commercial off-the-shelf components. EUV is unnecessary, enabling scalable manufacturing. Auto-calibration and low-frequency compensation suit low-power edge deployment.

Multi-mode writing and three erasability modes enable full-coverage production pathways:

- Single-shot area writing: low-cost, high-throughput mainstream computing.
- Depth-progressive writing: high-end industrial high-performance chips.
- Cross hybrid writing: flagship products with ultimate precision and yield.
- Three erasability modes configurable via UV parameters on one line, covering consumer, industrial, and secure markets.

All processes are backward-compatible; core area-source design preserves investment, with performance upgrades via pump modules only, enabling long-term evolution.

V3.50 further boosts production robustness: all-cold femtosecond-free processing eliminates microcracks and stress concentrations, zero thermal-stress failure, drastically improving batch consistency and long-term reliability.

#### 13 Industrial Innovation: Blank Medium Business Model and Computing Ecosystem Evolution

Supported by engineering feasibility and standard writing interfaces, B<sup>3</sup>D-HPA enables a paradigm-shifting business model that redefines data sovereignty and supply-chain structure, moving beyond the traditional vertical “design–manufacture–pack–preload” chip model.

Chip factories supply blank silica photonic substrates with standard programming interfaces only, with no preloaded programs, models, or fixed logic.

Blank media ship vendor-neutral, free of vendor-defined backdoors, data channels, or hidden services, providing only writable, calibratable, operable hardware. End users, enterprises, OEMs, and third-party developers locally inject models, algorithms, and logic via standard interfaces without cloud reliance, external connections, or exposure of computational intent or data.

This restructures the global computing industry at the physical layer:

### 13.1 Data Sovereignty From Promise to Physics

Mainstream digital security relies on vendor encryption, permissions, and policies: sovereignty is granted by suppliers. Even major platforms retain potential backdoor access, data exfiltration, updates, and remote control.

Under B<sup>3</sup>D-HPA's blank medium model, hardware is neutral at delivery; user-defined logic is written locally once, with no vendor involvement in runtime control. Index landscapes, PHAT mappings, and wavefield evolution are user-controlled and physically unreadable without in-person access. Security no longer depends on ethics or regulation but on photon confinement and medium locality, achieving true user data sovereignty.

### 13.2 Evolution of Computing Deployment

Cloud computing's business foundation rests on centralization, data upload, and platform control. Tech giants build moats via GPU clusters, APIs, and proprietary models. B<sup>3</sup>D-HPA enables independent, efficient, massively parallel edge physical computing. Blank media support flexible deployment: inference, training, rendering, optimization, and scientific computing locally without cloud submission. This enables an "edge-first, cloud-supplemented" model, coexisting with cloud services to drive decentralization and inclusive computing.

### 13.3 Industry From Vertical Integration to Open Collaboration

Traditional semiconductors suffer from design licensing, IP barriers, process monopolies, and ecosystem lock-in, causing concentration and exclusion.

B<sup>3</sup>D-HPA disaggregates the supply chain for open collaboration:

- Material suppliers: produce consistent, writable, calibratable blank media.
- Equipment makers: build standardized writing, reading, calibration tools.
- Software providers: offer writable algorithms, models, and applications.
- End users: full hardware control and logic definition.

Chips become general intelligent media, not locked proprietary products. Innovation shifts to developers and users, not fabs and cloud vendors, forming an open, fair, decentralized computing ecosystem.

### 13.4 Impact on Global Technology Balance

Industrialization offers a path to bypass silicon process restrictions, IP blocks, GPU monopolies, and cloud dominance, enabling direct advancement to next-generation storage-computing-integrated hardware. For regions constrained by sanctions, computing gaps, and security dependencies, B<sup>3</sup>D-HPA provides a viable route for

leapfrogging, autonomy, and foundational security. It rebalances global tech power: cloud centralization weakens, edge sovereignty strengthens, data and intelligence return to individuals and devices, advancing civilization from platform monopolism to inclusive openness.

#### 14 Conclusion

B<sup>3</sup>D-HPA V3.50 establishes a practically deployable dedicated continuous-wave optical computing acceleration architecture (OPU/TPU) centered on rare-earth phase lattices for sensing and anchoring, physical hash addressing for structural backbone, relative phase invariance for computing robustness, five-layer thermal drift mitigation for environmental stability, and cross hybrid writing for mass production.

It abandons perfect materials and uses architectural intelligence to neutralize physical imperfections.

It avoids computationally explosive inverse scattering and achieves ultra-low-power compensation via low-dimensional closed loops.

It replaces femtosecond ablation with all-cold dual-level locking for zero-stress, zero-drift, self-healing steady-state operation.

It supports fully erasable, bone-skin, and non-erasable modes for full-scenario coverage.

It overcomes 3D writing SNR and throughput limits via multi-mode hybrid integration, unifying mass production and precision.

It leverages the Effective Medium Theory (EMT) of rare-earth-doped silica to form boundaryless analog GRIN virtual waveguides, confining light and coupling modes, boosting coherent SNR and solving core engineering challenges while enabling dynamic reconfiguration and in-situ learning.

It provides standard optoelectronic interfaces for seamless integration with modern computing systems.

This architecture delivers a low-power, highly parallel, mass-producible, scalable hardware roadmap for the post-Moore era, moving continuous-wave optical computing from the lab to industry and real life, while providing a complete, implementable framework for 3D optical storage and computing.